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# Dale Beyer

## Expertise

High-speed ASIC design, validation, & verification. FPGA design. DSP algorithms, C, photonics, multiprocessor design, cache coherency, and PCI.

## Experience

2001-Present                      Chromadyne                      Beaverton, OR

### **Project Leader**

Led group responsible for the development of DSP algorithms used to mitigate the effects of linear and non-linear effects for a fiber optic transmission system.

- Investigation of Linear and Non-Linear effects in optical fiber.
- Developed a model of four-wave mixing in optical fiber.
- Characterized components in a optical fiber system.
- Developed Verilog for FPGA in an optical control loop.

1999-2001                      Geocast Network Systems                      Beaverton, OR

### **Senior Design Engineer**

Responsible for ATPG methodology and DSP development.

- Responsible for debug of ATSC playback and record system.
- Conducted research into ATSC reception quality and ghosting and developed software to measure and display realtime echos seen in recorded data.
- ATPG Methodology development for chip design flow, generated vectors for 3 chips.
- Used Chrysalis on custom cells to verify ATPG model is same as implemented version
- Responsible for the design of the Symbol loop development on a large satellite demodulator. Converted floating point model to fixed point version.

1997-1999                      Sequent                      Beaverton, OR

### **Intermediate System Engineer**

Developed ASIC and board level logic for the STiNG II.

- ASIC designer of IO section on ~1 million gate design.
- Tested and debugged basic functionality problems.
- Lead debug engineer in lab for early silicon validation of next generation baseboard STiNG II.
- Assumed Technical Project lead for baseboard of STiNG II.
- Used perl to design Verilog coding and baseboard routing tools.
- Knowledgeable in PCI, and several Intel proprietary buses.

